APPLICATION NOTE

- DEMOBOARD TDA8754 -
Universal Front End for Video and PC Graphics
Demonstration Board

AN/10295_1

VERSION 1.0

Philips
Semiconductors

PHILIPS

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SUMMARY

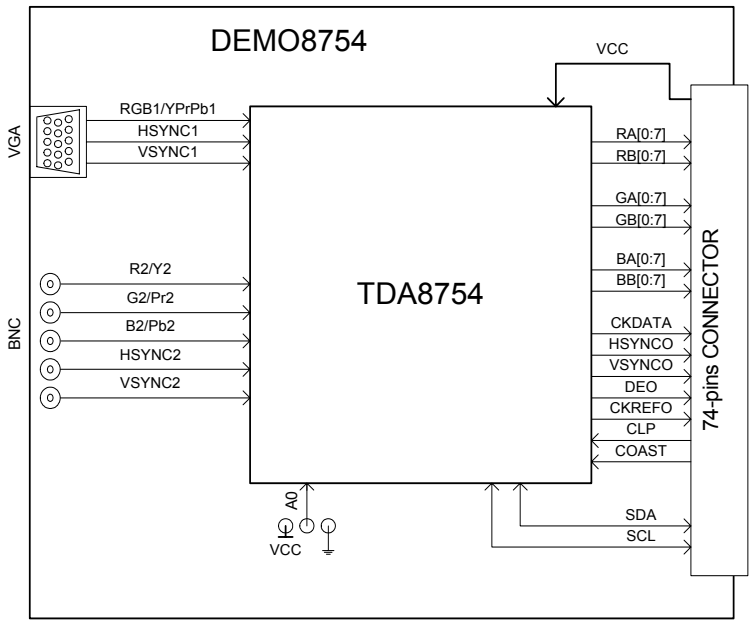
The TDA8754 is a complete triple 8-bit ADC with an integrated PLL running up to 270 Msps. This IC is optimized for capturing RGB or YUV video signals. It also has analog preprocessing functions like Programmable Gain Amplifier (PGA), blanking and internal generation of the clamp signal. The clamp level is programmable from code –24 to +136 in steps of 1 LSB. These functions are programmable independently for the three channels. The TDA8754 includes a 2:1 static selector which allows to choose between two analog video sources. It can also handle sync-on-green or composite signals thanks to a synchronization separator which can separate the composite sync information, whether it is a two level or three level sync. The line locked PLL uses as a reference input either an external horizontal synchronization signal, or the horizontal synchronization signal supplied by the internal sync separator circuit.

These functions allow the TDA8754 to be compatible with all TV and VESA standards up to 270 Msps pixel rate.

This **A**pplication **N**ote describes the design, the realization and the use of the **Demonstration Board TDA8754** (PCB n°1016-3).

1. PRINCIPLE AND DESCRIPTION OF THE BOARD:

The principle of the **Demo**nstration **Board** for the **TDA8754**, which is described in this **A**pplication **N**ote, is shown on **Figure 1**.



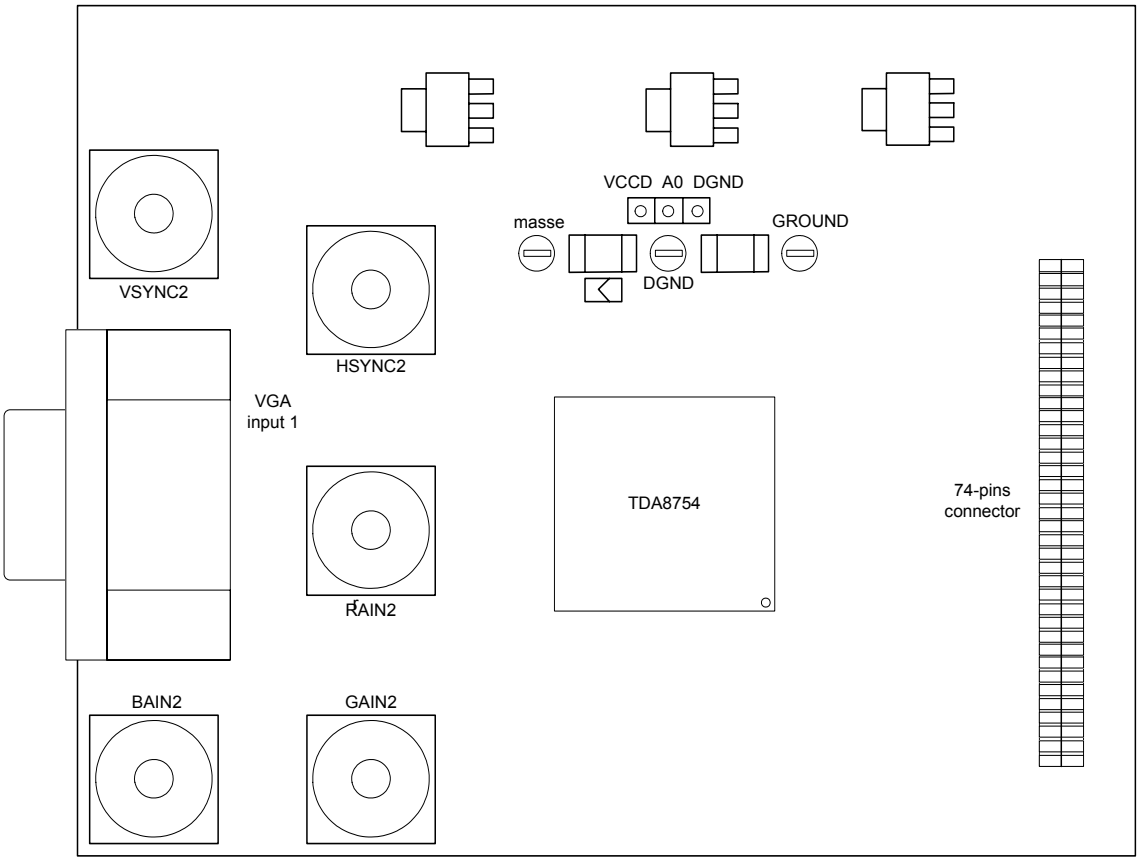
- Figure 1. Block diagram of Demoboard -

The different blocks of the **Demoboard** are:

- One video connector (**VGA**) to connect a video source (PC, DVD player, pattern generator…)
- 5 **BNC connectors** to connect a second video generator
- A **74-pins connector** to output digitized data, synchronization pulses and other signals generated by the TDA8754 or to receive control signals.
- The **5 V** power supply of the demoboard, provided thru the 74-pins connector. 3 regulators convert the 5V in 3.3 V and supply the TDA8754 on the board.
- The **I2C-bus** to control the TDA8754, coming from the 74-pins connector.
- One switch (**A0)** to choose the TDA8754 I2C address.

2. OVERVIEW OF THE BOARD:

The overall implantation of the **Demoboard** is shown on **Figure 2**.



- Figure 2. Overview of Demoboard -

The different connectors, jumper and test points available on the board are:

- **For the general power supply:**

1. The **+5V$_{DC}$** is provided by the main board. There is no connector on this board to supply directly the TDA8754.
2. There are three ground connections **GROUND, MASSE** and **DGND** respectively for output, analog and digital ground.

- **For the connection to video sources:**

1. One **VGA** connector for the first analog input.
2. Five **BNC** connectors for the second analog input (YPbPr or RGB and synchronization signals, if needed).

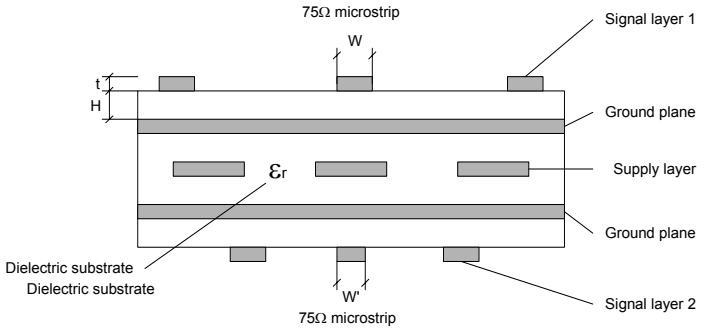
- **The I2C-bus** is not accessible directly on this board. The TDA8754 can only be addressed thru the 74 pins-connector.

- **For the output, a** 74**-pins connector** SAMTEC SMS_137_02_TD to output all signals generated by the TDA8754. There is also on this connector the 5V power supply, the I2C-bus, the clamp and the coast signals.

- **The jumper A0** to select the I2C slave address of the TDA8754.

3. PCB DESIGN:

The design is made on a multilayer **P**rinted **C**ircuit **B**oard. The technological concept used to make this PCB is given on **Figure 3**.



- Figure 3. PCB structure -

Five physical copper layers are used. The top and the bottom layers are the signal layers that contain the 75Ω micro strips. The second and fourth layers constitute the ground planes corresponding to the signal layers. And the third layer situated between the two ground planes has been provided especially to design the power wiring system.

The dielectric substrate is an Epoxy Glass resin with a relative permittivity (ε_r) of 4.4 and a thickness (H) of 175 μm between the signal layers and the ground planes. The copper thickness (t) of the external layers is 47 μm and the global thickness of the PCB is about 1.6 mm. The metallic hole technique is employed to make all the necessary interconnections between the layers.

3.1 CONTROLLED IMPEDANCE MICROSTRIPS:

The analog lines **B/V**, **G/Y**, **SOGIN** and **R/U** must be adapted to 75Ω. These adaptations are made with the microstrip method. The widths W and W' were calculated with the software "Polar Si6000 Controlled Impedance Quick Solver" from Polar Instruments (www.polarinstruments.com).

To obtain 75 Ω lines, width **W' = 120 μm** was chosen.

3.2 POWER SUPPLY WIRE:

To avoid ground plane discontinuities of the line technological structure, the supply wiring system of all circuitry has been made on the internal third layer. Moreover, in order to reduce the voltage fluctuation effects due to switching currents inside the different integrated circuits devices, the power supply wires are designed with a low characteristic impedance of microstrip lines in order to obtain a small equivalent inductance.

3.3 ANALOG AND DIGITAL RETURN GROUND POINT:

To minimize the noise due to capacitive coupling between the analog, output and the digital parts of the TDA8754, three separate ground planes are designed on all layers and are connected together through an inductor.

3.4 PLL FILTER (CP, CZ)

The most critical point for the PLL is the external loop filter. The capacitances Cp (680 pF) and Cz (220 nF) must be as close as possible to the TDA8754. It is important to minimize the length of the wires.

4. OPERATING MODE:

This TDA8754 Demoboard cannot be used alone. It has been designed to be plugged in **two kinds of application systems**:

- Demonstration application more dedicated to high frequency.
- Evaluation kit, dedicated to low frequency (less than 110 MHz).

4.1 DEMONSTRATION APPLICATION:

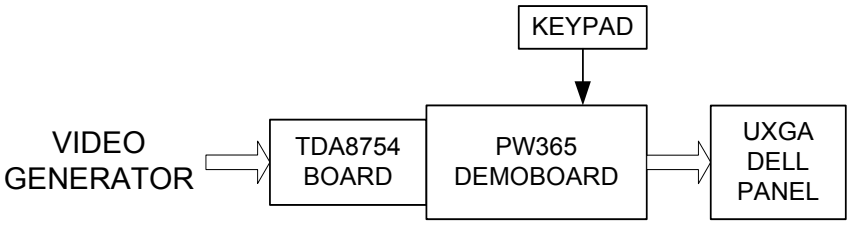
The first thing to verify in case of "*demonstration application*" is the position jumper A0. It must be on VCCD. In that case the TDA8754 I2C address is 9A.

The demonstration board can then operated up to 240 Mhz. It consists of the TDA8754 demoboard connected to the Pixelworks (PW365) demoboard. And the total set is connected to a DELL 20 inches UXGA panel.

The software available to drive this application is embedded. It is working automatically whatever is the input. In case of problem, a reset button is available on the Pixelworks board.

A remote control (or a keypad) is available to change some parameters. For example, PLL phase step, brightness (=ADC clamp), contrast (=ADC gain) and PLL divider may be adjusted.

This set is available in several Philips offices (Asia, Europe and the USA) and can be borrowed on request.



4.2 EVALUATION KIT:

When in "*evaluation kit mode*", the first thing to check is the position of the jumper A0. It must be on DGND. In that case the TDA8754 I2C address is 98.

This kit is more dedicated to the TDA8754 evaluation in low frequency (less than 110 MHz).

There are three boards to connect together: TDA8754, INTPWDVI and INTDVI. The output of this kit is a DVI transmitter. It may be connected to any DVI receiver via a DVI cable.

The INTPWDVI board generates the vertical data enable, has an I2C input connector and manages the power supply. Its main role is to interface the TDA8754 demoboard with the INTDVI board.

The INTDVI board has the function to format and transmit data in DVI format. It consists of a DVI transmitter IC, some supply regulators and switches and a DVI output connector.

An I2C cable must be connected to the INTPWDVI board to drive TDA8754 registers.

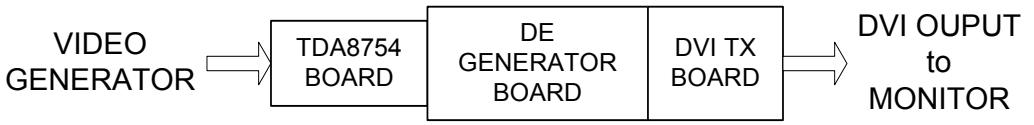
The software to drive the kit is called URD (Universal Register Debugger). This software developed by Philips is free and can be installed on any computer. The kit may not be used without this software.

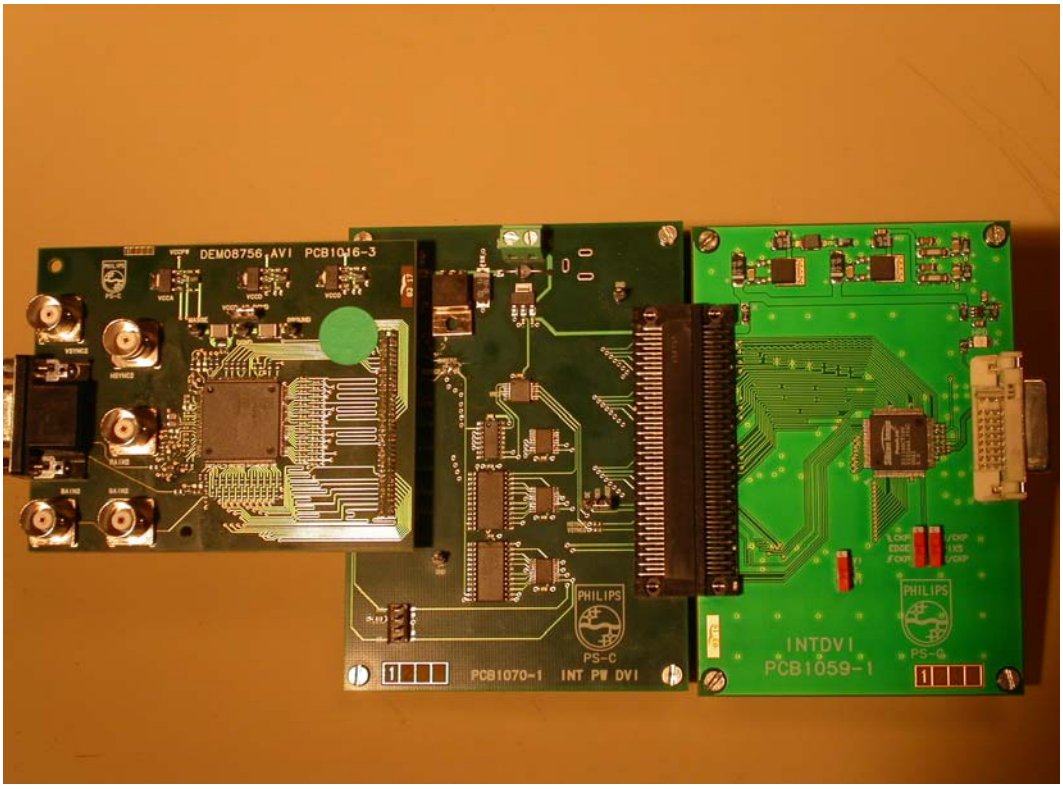
The first thing to do is to supply the INTPWDVI board with a 9V power supply. The whole kit is supplied with this single supply. Then you must connect the I2C cable between the computer and INTPWDVI board. Launch the URD software. Load the .urg file. It is ready to run.

Each time a new standard is input in TDA8754 or if there is any change in the input, the .urd file corresponding to this standard must be loaded in the URD software.

It is possible to change all TDA8754 I2C register values in the URD software. It allows to test all functionalities.

The evaluation kit boards are available on request. They are delivered with all switches properly positioned for correct operation. Register mappings for many formats, to be uploaded with the URD software, are also available on request and can be sent by email.





EVALUATION KIT

5. LAYOUT ADVICE:

As the TDA8754 is a high-speed analog device, it is important to follow this guide for designing a board.

It is recommended to decouple all **supply pins** with a 100 nF capacitor. If two supply pins of the same type are close and if there is not enough space on the PCB, it is allowed to use only one decoupling capacitance.

It is important to have a very low noise on power supply pins. It is preferable to have separate regulated supplies for analog/digital and output worlds. Analog/digital supply pins are $VCCA_{(X)}$, $VCCD_{(X)}$. Output supply pins are $VCCO_{(X)}$.

It would be also good for PLL jitter to have another regulator dedicated to the PLL supply pin (VCCAPLL).

It is recommended to use a minimum of two **ground planes** : one for the analog/digital world and one for the output world. The two planes must be connected on a single point thru an inductance. The analog ground plane, analog trace and the analog supply plane must be superimposed. The same rules apply for output planes.

One of the most critical points concerning the PLL layout is the place of the capacitances **Cp and CZ**. It is very important to have them as close as possible to the TDA8754 and on the same layer if possible. Values of these capacitances indicated in the datasheet must not be changed. It is also important for the stability of the PLL to avoid parasitic components or wires close to this filter.

Another critical wire for the PLL jitter is **HSYNC1** (or CHSYNC1 or SOGIN1) for input 1 or **HSYNC2** (or CHSYNC2 or SOGIN2) for input 2. It is also interesting to have a short trace length and a less noisy environnement to optimise the PLL jitter.

All **input pins which are not used** must be grounded (except SOGIN). For example, if coast is not used, internal PLL is used and an external clamp is provided, then the following pins should be grounded: TEST, TCK, ACRX1, ACRX2, CKEXT, COAST... It also means that if there is only one video input used, the not used video port input must be directly connected to ground.

If SOGIN1 input (or SOGIN2 input) is not used, the pin must be grounded thru a 330 pF capacitance.

Concerning **video input**, 75 ohms termination resistors must be as close as possible to the TDA8754. It is important to have adapted 75 ohms line for the 3 video input signals to avoid reflection. The length of the input traces should be the same and as short as possible. As explained before for the PLL, it is important not to have digital or output signals (which are noisy) in the same area.

All **not used output pins** must always be left open (For example: CLPO, FIELDO, HPDO, ROR…).

It is also better to have the same trace lengths for all **output data and clocks**. It will avoid timing problems due to output load differences. It is also better to have these traces as short as possible.

If the **TDA8754 video input** is **directly connected to the video input connector**, it may happen that there is a video signal in the input of the TDA8754 although the circuit is not powered. If this case could happen in the application, pins

Hsync and Vsync must be protected with 220 ohms resistors in series. These resistors should be as close as possible of the input pins and after the 75 ohms adaptation resistor.

6. USE ADVICE

Concerning the clamp, it is preferable to use the internally generated clamp pulse (register 15h, CLPSEL2 = 0), generated with the pixel counter. It will avoid some timing issue. To use this internal function, registers Hsyncl, Hbackl and Hdispl must be well programmed.

For the same reason, it is better to use Hsynco output instead of Ckrefo output.

When Hsynco is used, for a good start up in a final application, as the pixel counter is not well programmed, the Hsynco should come from the sync separator (register 15h, HSOSEL=1). After the start up phase, when the input standard has been detected by a scaler or a microprocessor, and all TDA8754 PLL and pixel counter registers have been well programmed, HSYNCO must come from the internal pixel counter (register 15h, HSOSEL=0).

When the TDA8754 is programmed in dual output mode (=demux mode, register 17h, bit DMXRGB=1), the Hsyncl, Hbackl and Hdispl registers values must be even to have a correct output timing (DEO,HSYNCO). If a one pixel shift is needed in demux mode, the bit Schckrefo must be used.

7. DEMOBOARD FILES:

The signals on the 74-pins connector are given on **Table 1**.

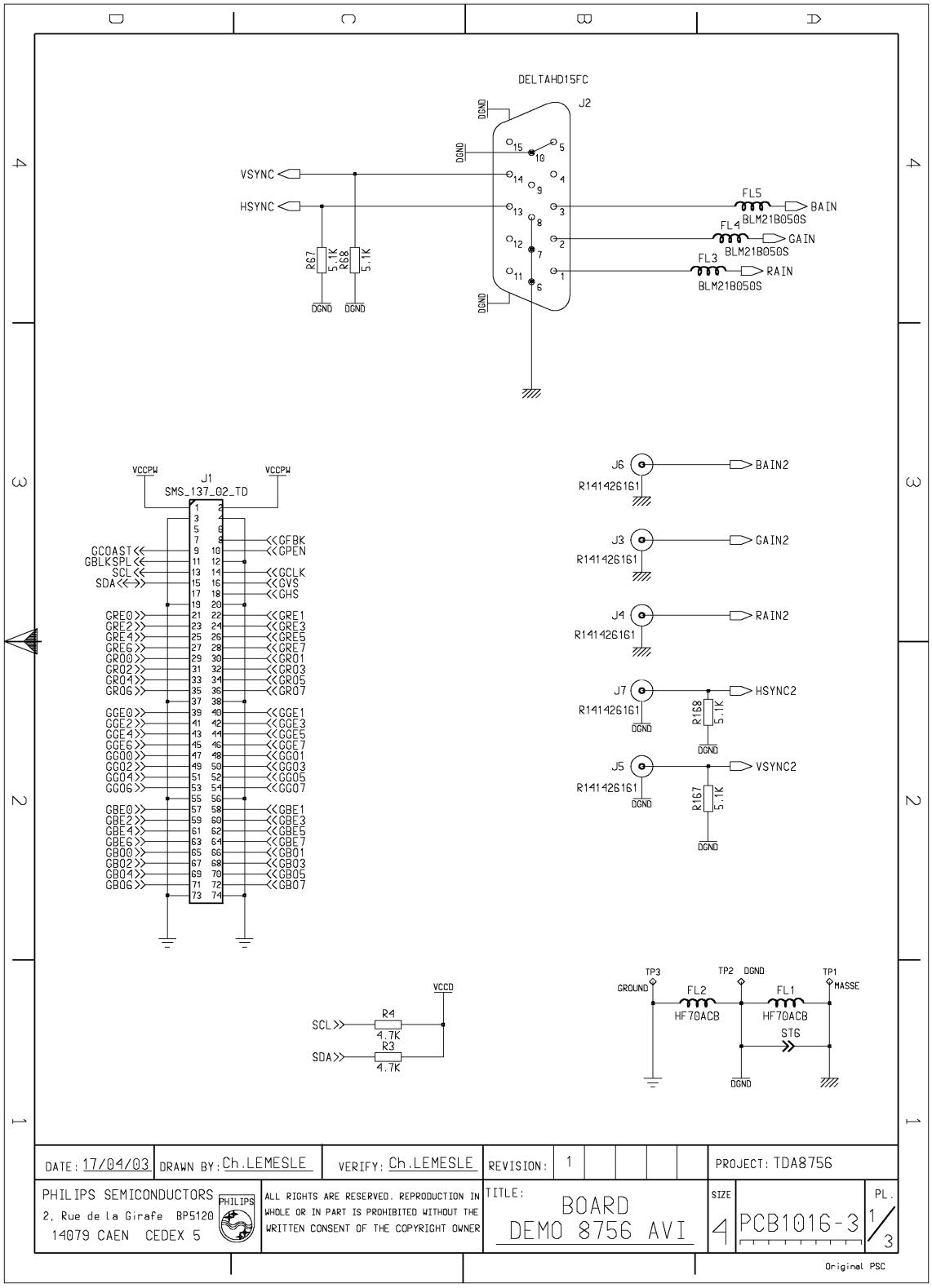
All documents needed for the realization of this Demoboard are given on **Figures 5 to** 12.

- Electrical diagram.
- Topside component implantation.
- Underside component implantation.
- Topside signal layout.
- Internal ground plane layout.
- Internal supply layout.
- Underside signal layout.

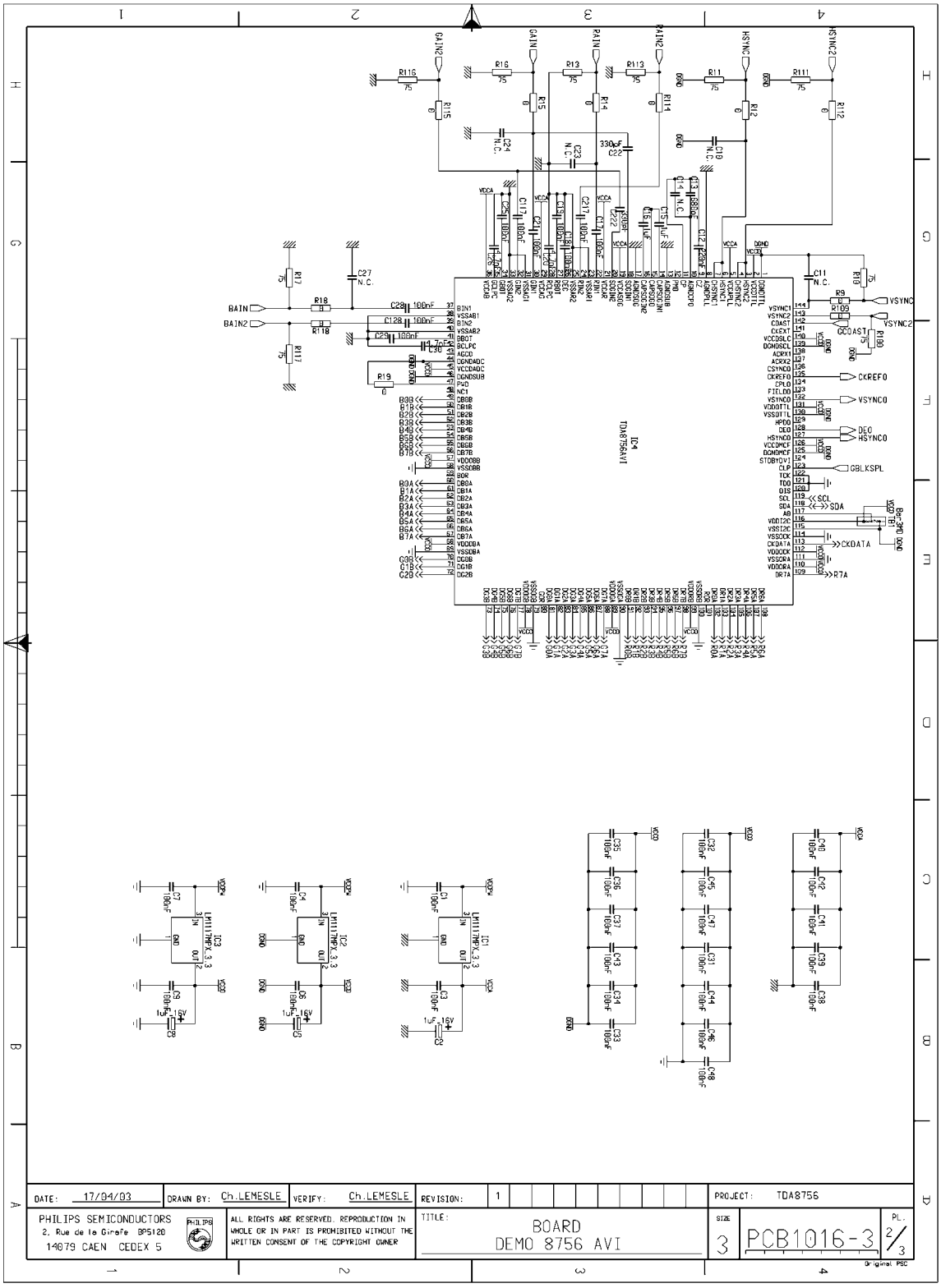
The components list with their values and references is given on **Table 2**.

5 V	1	2	5 V
DGND	3	4	DGND
NC	5	6	NC
NC	7	8	CKREFO
COAST	9	10	DEO
CLAMP	11	12	DGND
SCL	13	14	CKDATA
SDA	15	16	VSYNCO
NC	17	18	HSYNCO
DGND	19	20	DGND
R0A	21	22	R1A
R2A	23	24	R3A
R4A	25	26	R5A
R6A	27	28	R7A
R0B	29	30	R1B
R2B	31	32	R3B
R4B	33	34	R5B
R6B	35	36	R7B
DGND	37	38	DGND
G0A	39	40	G1A
G2A	41	42	G3A
G4A	43	44	G5A
G6A	45	46	G7A
G0B	47	48	G1B
G2B	49	50	G3B
G4B	51	52	G5B
G6B	53	54	G7B
DGND	55	56	DGND
B0A	57	58	B1A
B2A	59	60	B3A
B4A	61	62	B5A
B6A	63	64	B7A
B0B	65	66	B1B
B2B	67	68	B3B
B4B	69	70	B5B
B6B	71	72	B7B
DGND	73	74	DGND

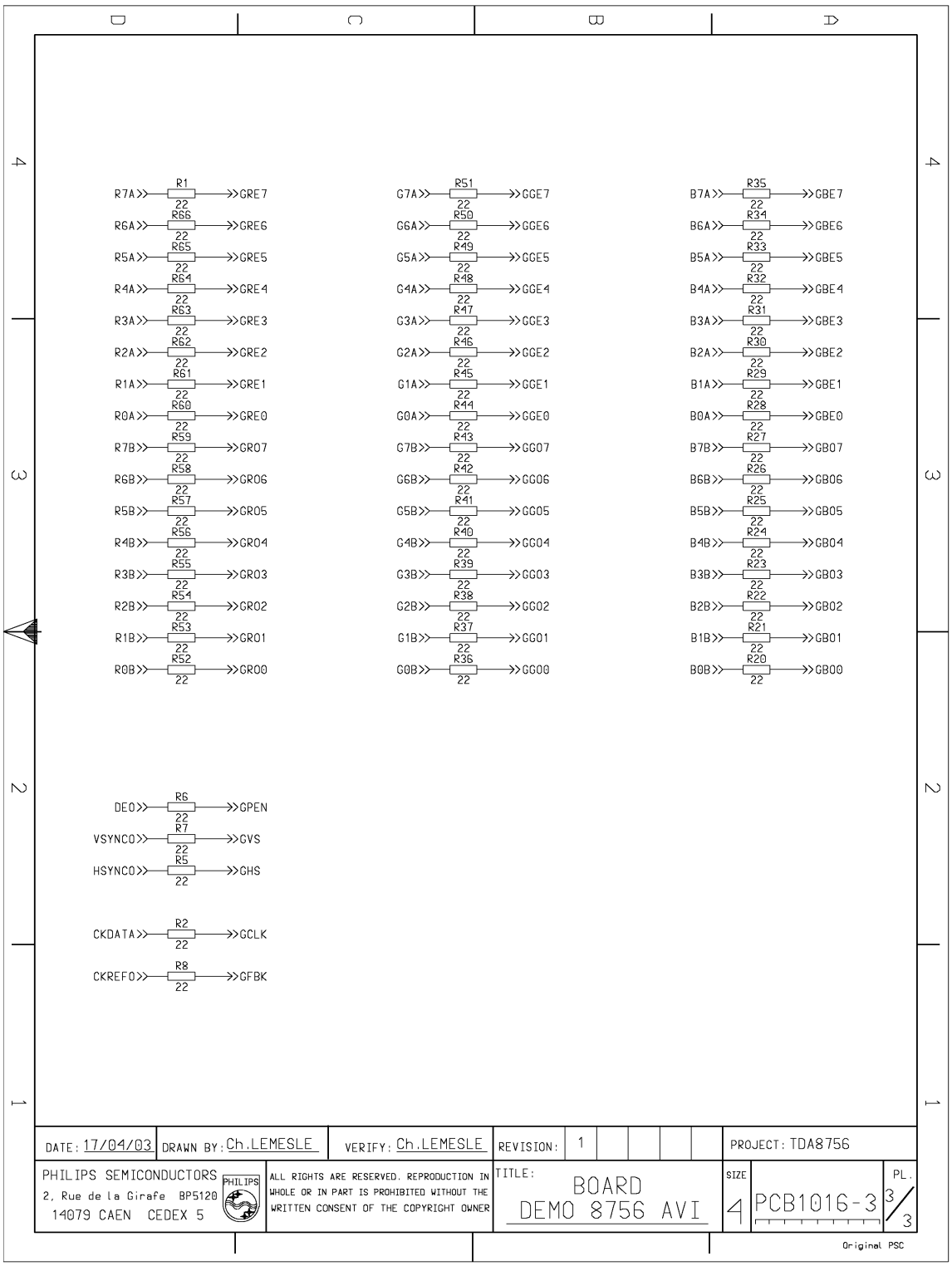
- Table 1. DEMOBOARD TDA8754 74-pins output connector -



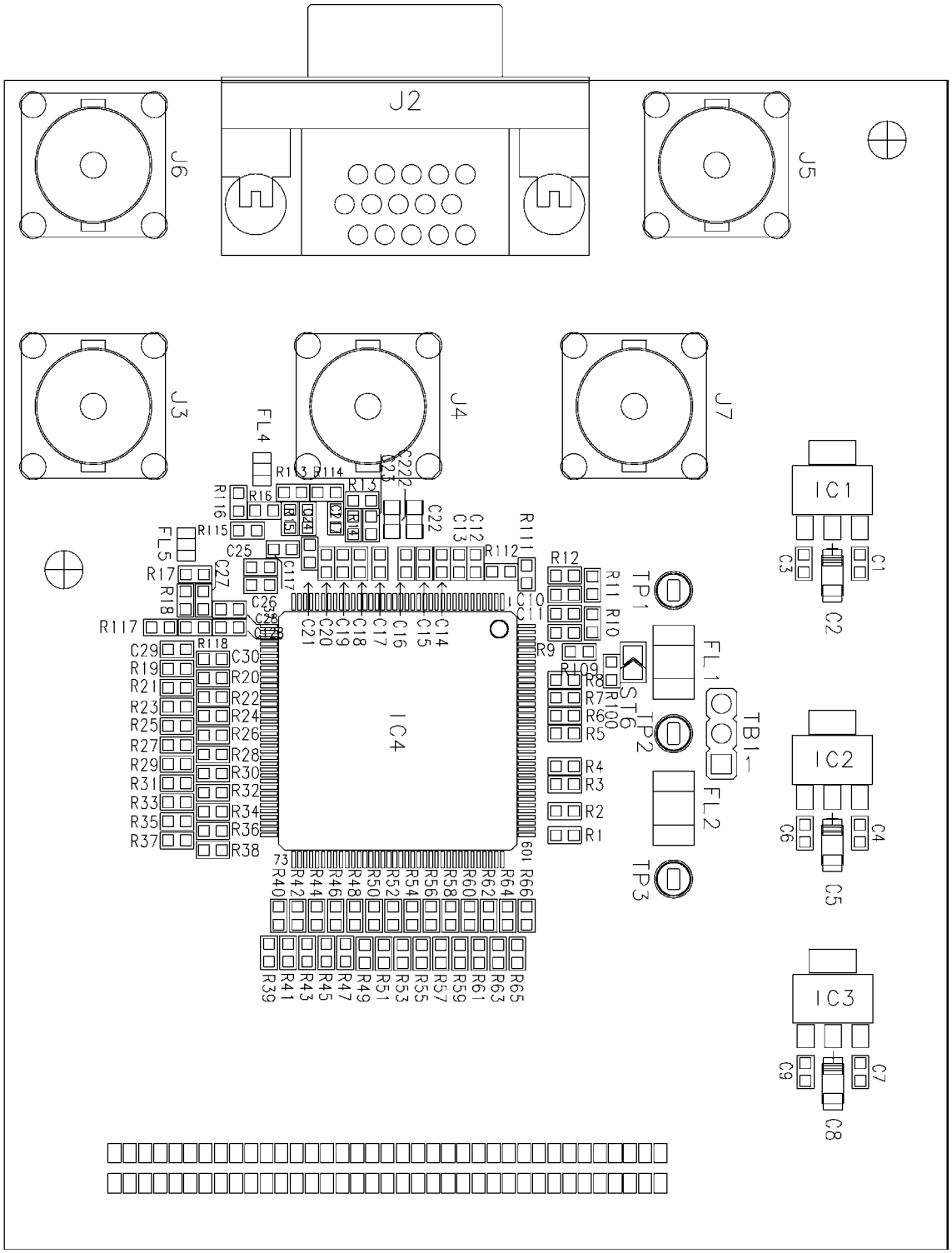
- ***Figure 4. DEMOBOARD TDA8754 electrical diagram (Page 1)-***



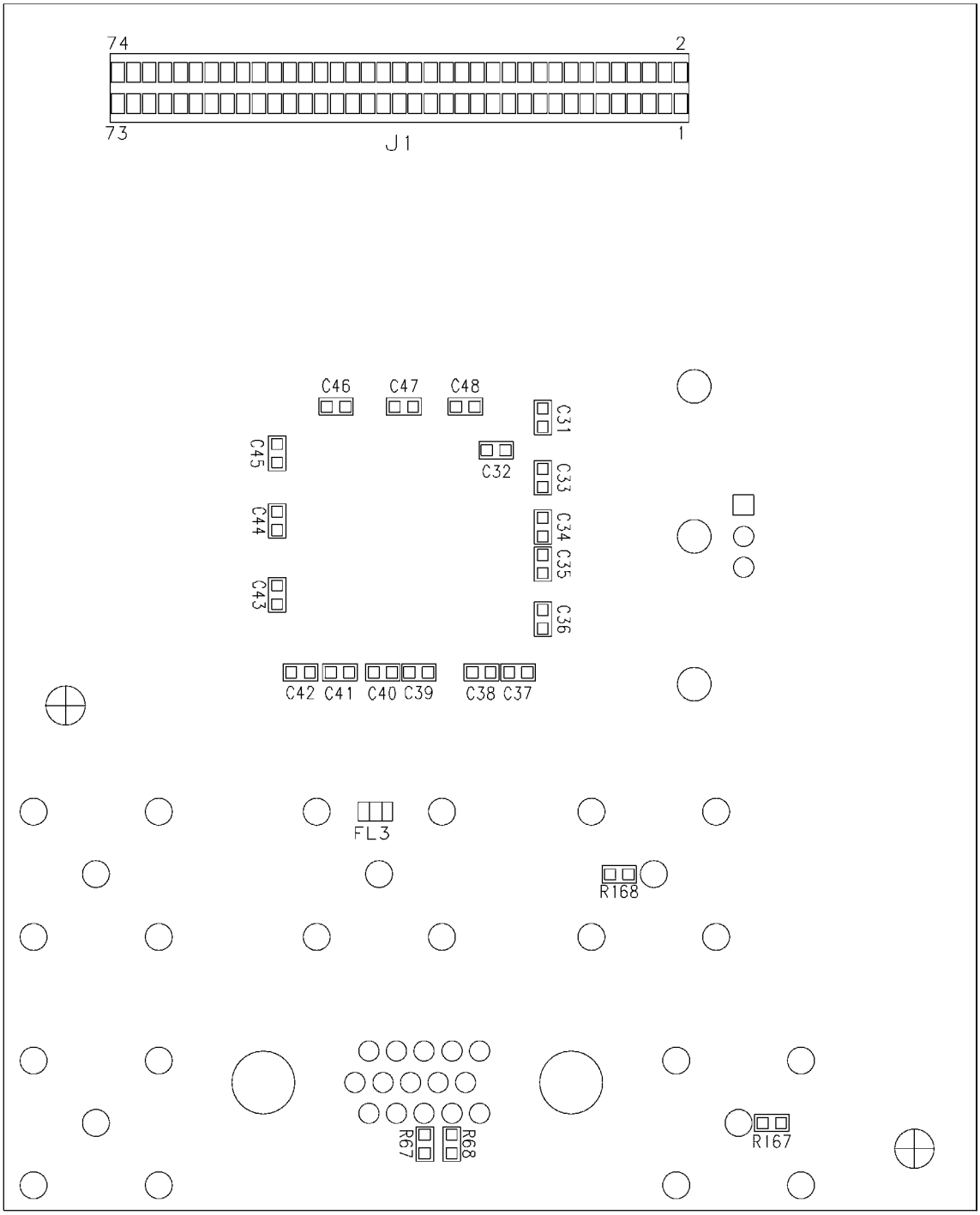
- ***Figure 5. DEMOBOARD TDA8754 electrical diagram (Page 2)-***



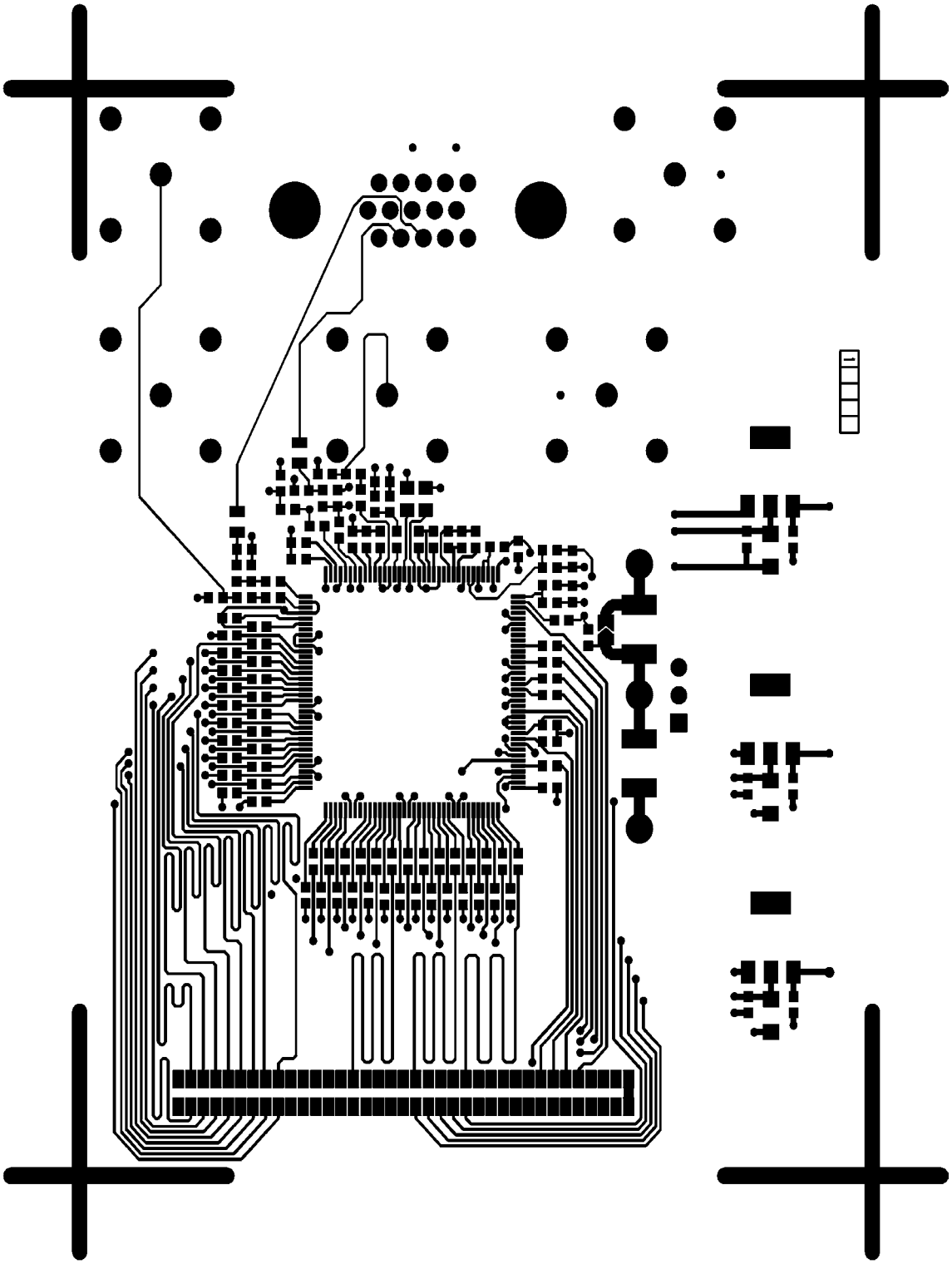
- ***Figure 6. DEMOBOARD TDA8754 electrical diagram (Page 3)-***



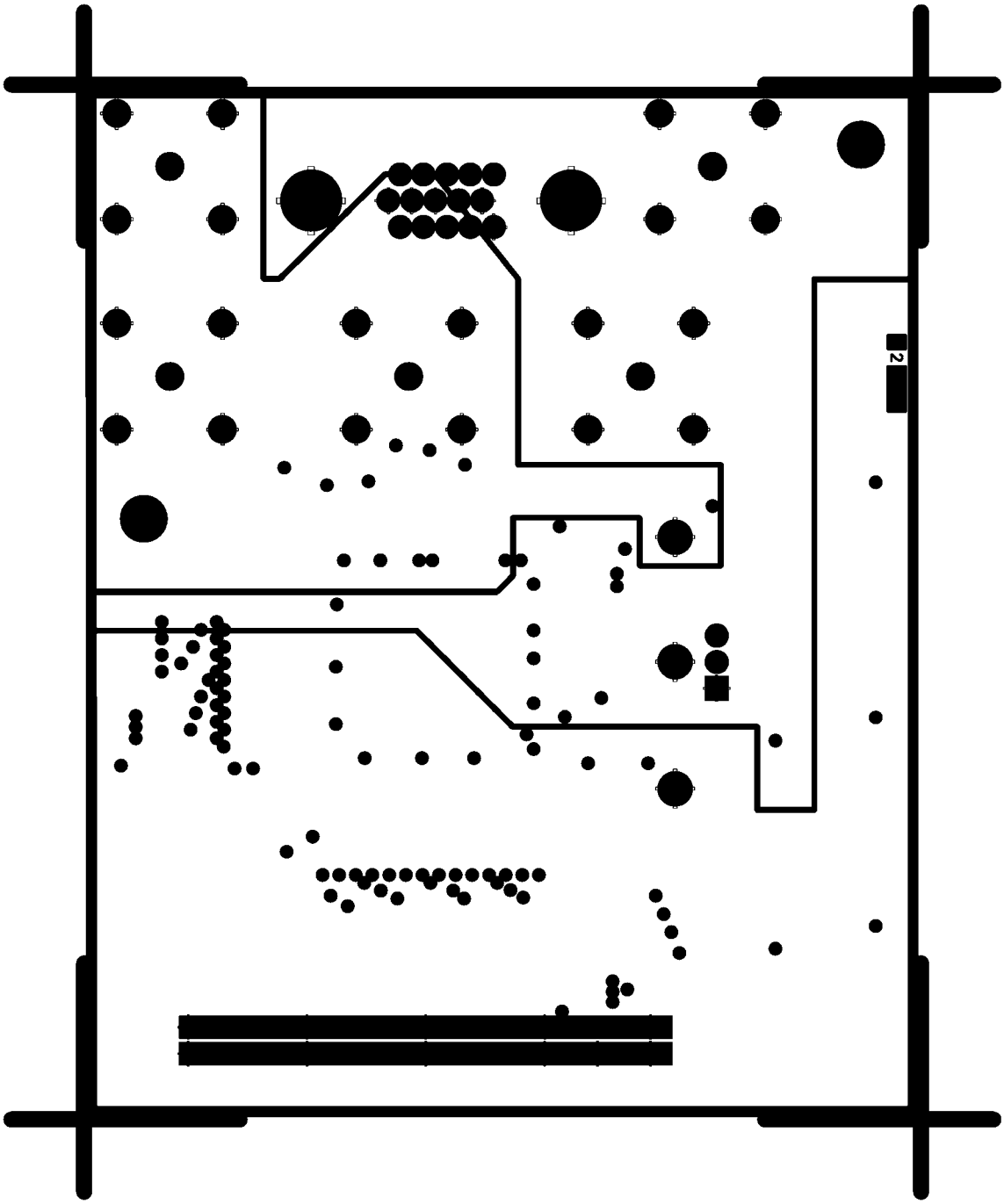
- Figure 7. DEMOBOARD TDA874 topside component implantation -



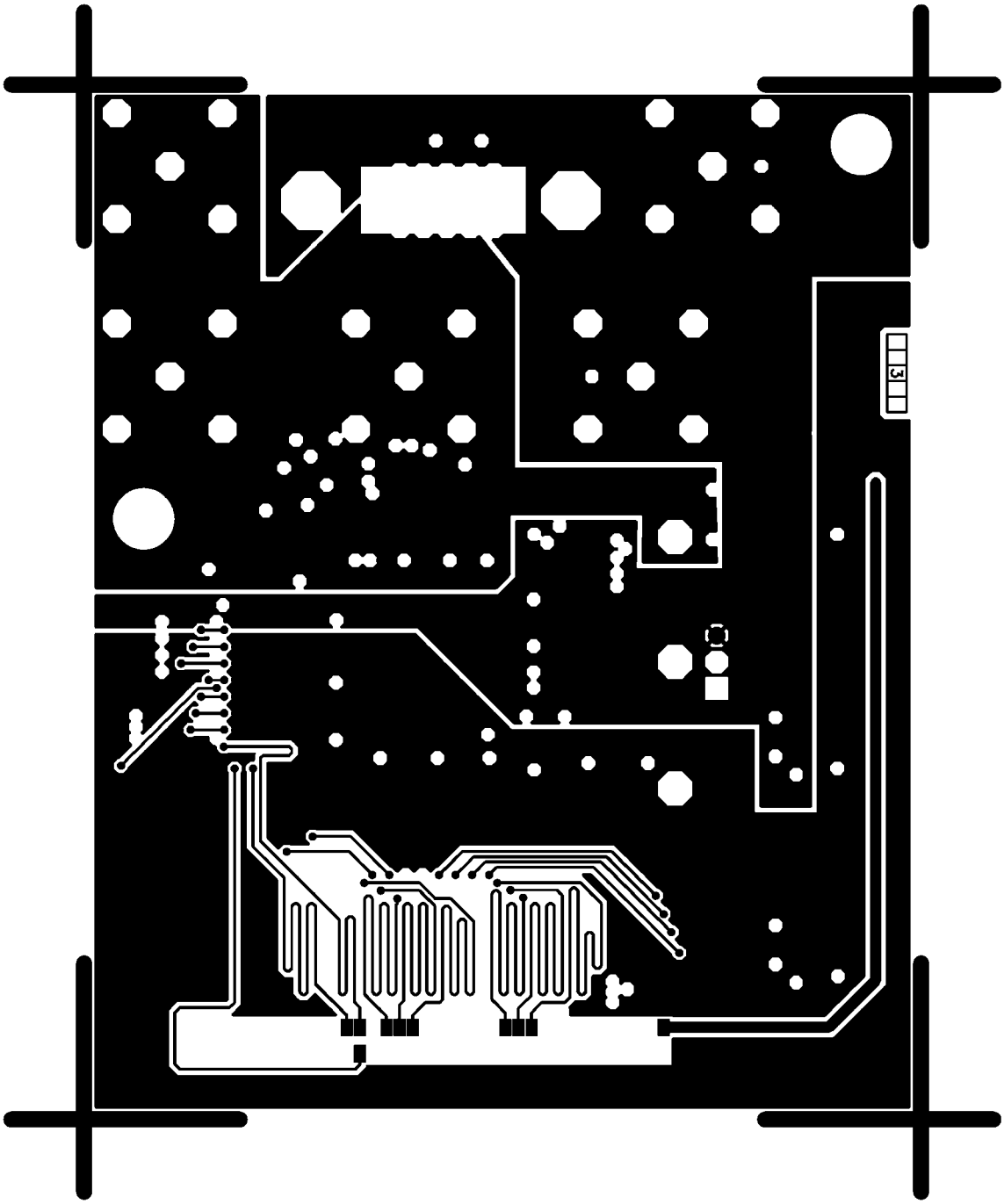
- Figure 8. DEMOBOARD TDA874 underside component implantation -



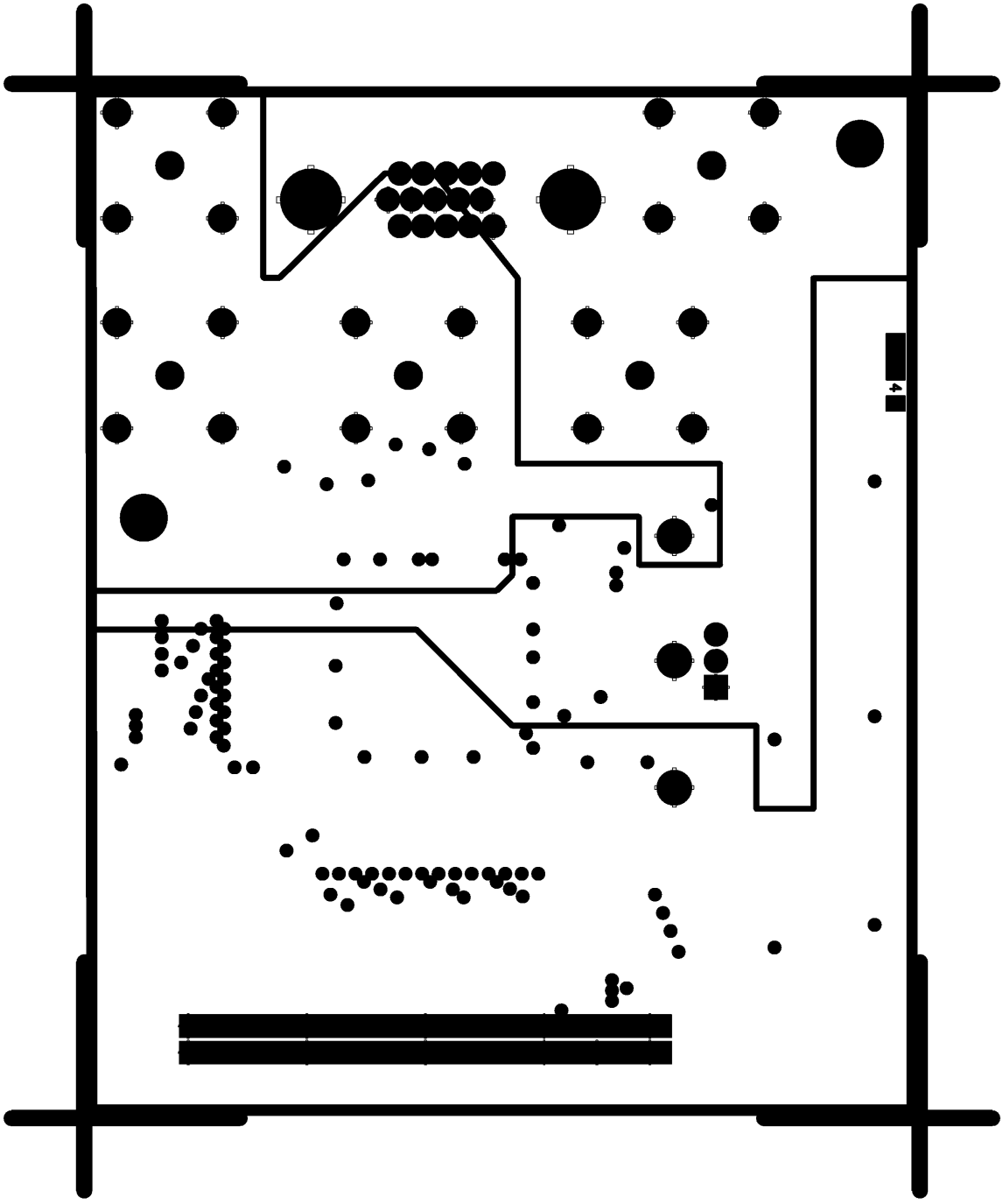
- Figure 9. DEMOBOARD TDA8754 topside signal layout (layer 1) -



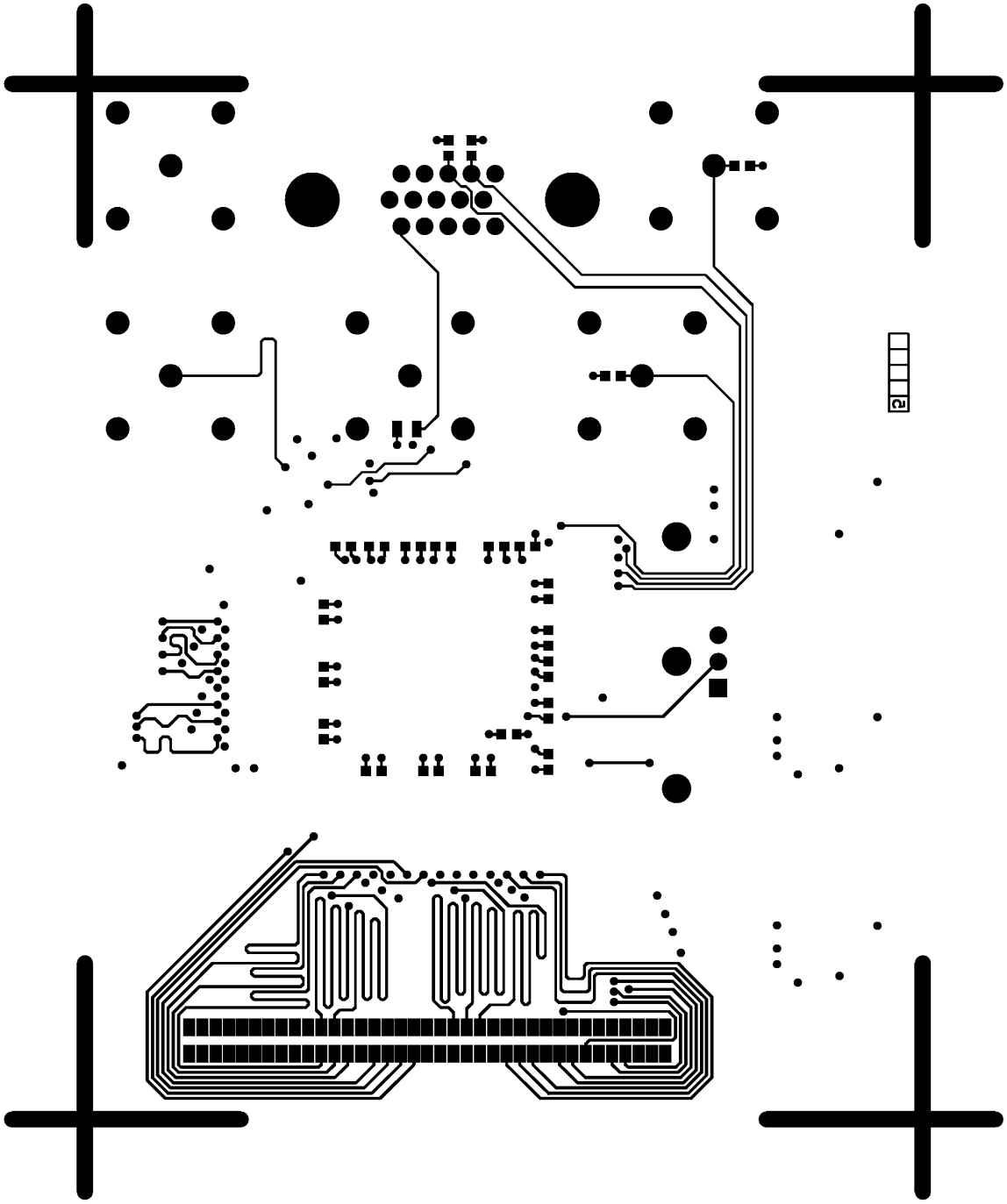
- Figure 10. DEMOBOARD TDA8754 internal ground plane layout (layer 2) -



- Figure 11. DEMOBOARD TDA8754 internal supply layout (layer 3) -



- Figure 10. DEMOBOARD TDA8754 internal ground plane layout (layer 4) -



- Figure 12. DEMOBOARD TDA8754 underside signal layout (layer 5) -

REF	VALUE	COMPONENT	TYPE	MANUFACTURER
C2, C5, C8	1µF/16V	Capacitor	293D/A	
C15, C16	1uF	Capacitor	0603	
C12	220nF	Capacitor	0603	
C1, C3,C4,C6,C7,C9, C17, C18,C19,C21,C25,C28, C29,C31,C32,C33,C34, C35,C36,C37,C38,C39, C40, C41,C42,C43,C44, C45,C46,C47,C48,C117, C128,C217	100nF	Capacitor	0603	
C20, C26, C30	4,7nF	Capacitor	0603	
C13	680pF	Capacitor	0603	
C22, C222	330pF	Capacitor	0603	
FL1,FL2	HF70ACB	Filter	1812	
FL3,FL4,FL5	BLM21B050S	Filter	BLM21	TUSONIX
IC1, IC2,IC3	LM1117MPX_3.3	Voltage Regulator	SOT223	NS
IC4	TDA8754HL	ADC Converter	SOT486_1	PHILIPS
J1	SMS_137_02_TD	Connector	Sms2x37_1.27fd	SAMTEC
J2	DELTAHD15FC	Connector		
J3,J4,J5,J6,J7	Bnc_d	Connector	Female	RADIALL
R67,R68,R167,R168	5.1K	Resistor	0603	
R3,R4	4.7K	Resistor	0603	
R10,R11,R13,R16, R17, R100,R111,R113,R116, R117	75	Resistor	0603	
R1,R2,R5,R6,R7,R8,R9, R20,R21,R22,R23,R24, R25,R26,R27,R28,R29, R30,R31,R32,R33,R34, R35,R36,R37,R38,R39, R40,R41,R42,R43,R44, R45,R46,R47,R48,R49, R50,R51,R52,R53,R54, R55,R56,R57,R58,R59, R60,R61,R62,R63,R64, R65,R66	22	Resistor	0603	
R12,R14,R15,R18,R19, R109, R112, R114, R115, R118	0	Resistor	0603	
ST6		Jumper		
TB1	Bar3MD	Single Row		
TP1,TP2,TP3	5011	Test Point		KEYSTONE

Table 2. List of components